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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/556,005	11/08/2005	Atul Katoch	NL 030576	5020

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER

WHITE, DYLAN C

ART UNIT	PAPER NUMBER
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2819

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/556,005

Applicant(s)

KATOCH ET AL.

Examiner

Dylan White

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 November 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-10, 13 and 14 is/are rejected.
- 7) ☒ Claim(s) 7, 11 and 12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 November 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

The abstract of the disclosure is objected to because it is not on a separate sheet of paper. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: The Specification should include the following headings (the Examiner has picked the locations in the specification believed to be the division between each section);

Page 1, line 2: Field of invention

Page 1, line 5: Background of the Invention

Page 2, line 16: Summary of the Invention

Page 3, line 3: Brief Description of the Drawings

Page 3, line 28: Detailed Description of the Preferred Embodiments

Page x, line x: Conclusion (if necessary)

Appropriate correction is required.

Drawings

The drawings are objected to because Figure 7 is too condensed to see each specified signal at the times between 1-3ns and 5-6ns. The Examiner suggests either expanding Figure 7 (if possible) to provide one with the ability of differentiating the five

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different signals or separating the signals on more than one stacked graph where signals can be view concurrently over the same time and voltage scale (the Examiner has provided and example of this for clarity).

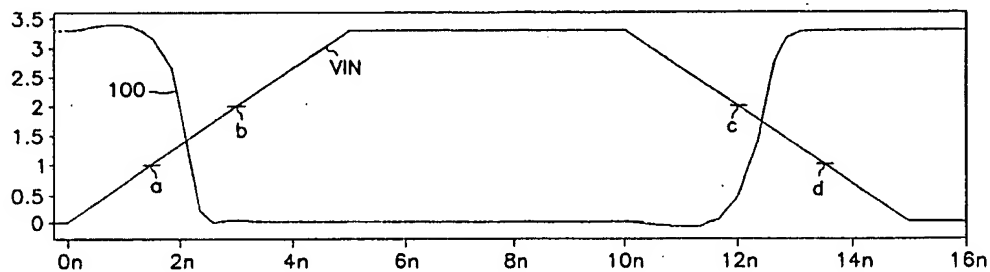


Fig. Xa

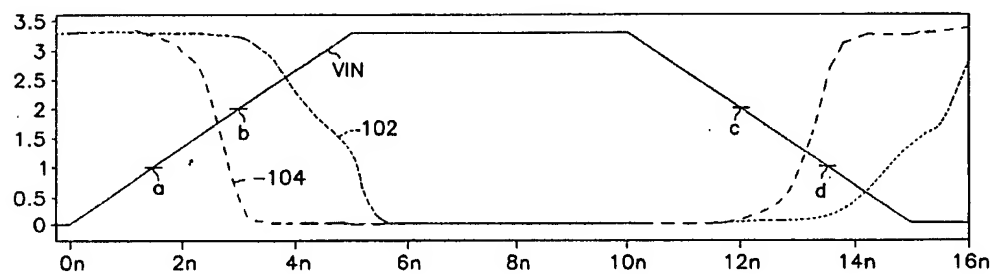


Fig. Xb

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

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consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1-15 are objected to because of the following informalities: Claims shall not contain reference numbers/descriptors. Appropriate correction is required.

Claim 10 is objected to because of the following informalities: in line three it states "the gate of p-mos device being controlled by the input signal" the examiner believes the claim should state it as "the gate of the first p-mos device". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8, and 15, are rejected under 35 U.S.C. 102(b) as being anticipated by Wright et al. (US Pat. 5,612,630).

Regarding claim 1, Wright discloses a buffer circuit (22 @ Fig. 1) receiving an input signal (V_{in}) and producing an output signal (V_{out}), and comprising a first (52 & 58) and second (30) inverter stages, characterized in that the buffer circuit (22) comprises means (50, 54, 56, and 60) for dynamically controlling the switching threshold of the first inverter (52 & 58) stage according the state of one or more aggressor signals (input to transistors 54 & 60).

Regarding claim 8, Wright discloses where the means (50, 54, 56, and 60) for dynamically controlling the switching threshold comprises means for selectively controlling a pull up path (V_{dd} side) and/or a pull down path (GND side) of the first inverter (52 & 58) stage.

Regarding claim 15, Wright discloses receiving an input signal (V_{in}) and producing an output signal (V_{out}) using first (52 & 58) and second (30) inverter stages, being characterized by dynamically controlling the switching threshold of the first inverting stage (52 & 58) according to the state of one or more aggressor signals (input to transistors (54 & 60)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-6 and 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (US Pat. 5,612,630) in view of Keeth (US Pat. 5,917,758).

Regarding claim 2, Wright discloses the buffer of claim 1 where means (50, 54, 56, and 60) for dynamically controlling the switching threshold receives a first aggressor signal (to transistors 54 & 60) for controlling the switching threshold.

Wright fails to disclose a second aggressor signal.

Keeth discloses an adjustable output driver where adjustable circuit (322) has means (338b-x) for dynamically controlling the switching threshold of a first inverter (transistors 334 & 336) with a first (340b/344b, shown but not labeled) and second (340x/344x) aggressor signals for controlling the switching threshold, therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the buffer disclosed by Wright with the switching means as taught by Keeth for controlling the slew rate of the input signal.

Regarding claim 3, the combination discloses where the means (Wright, 50, 54, 56, and 60 @ fig. 1) for dynamically controlling the switching threshold comprise means for lowering the switching threshold when the signal wire (Vin) is in a first logic state

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(high) and the first and second aggressor signals (340b/344b & 340x/344x) are at a second logic level (low).

Regarding claim 4, the combination discloses where the switching threshold is lowered by lowering the switching voltage of the first inverting stage (Wright, 52 & 58 @ Fig. 1) when the signal wire (Vin) is at a low logic level (Vin = low, aggressor signals = high).

Regarding claim 5, the combination discloses where the switching threshold is lowered by lowering the switching voltage of the first inverter stage (Wright, 52 & 58 @ Fig. 1) when the signal wire (Vin) is at a high logic level (Vin = high, aggressor signals = low).

Regarding claim 6, the combination discloses where means (Wright 50, 54, 56, and 60) for dynamically controlling the switching threshold comprises means for raising the switching threshold when the signal wire (Vin) and the first and second aggressor signal (340b/344b & 340x/344x) are at the same logic level (Vin = high, aggressor signals = high).

Regarding claim 8, the combination discloses where the means (50, 54, 56, & 60) for dynamically controlling the switching threshold comprises means for selectively

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controlling a pull-up path (50 & 54) and/or pull-down path (56 & 60) in the first inverter stage (52 & 58).

Claims 9-10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (US Pat. 5,612,630) in view of Keeth (US Pat. 5,917,758) in further view of Patel et al (US Pat. 6,433,585)

Regarding claim 6, the combination discloses that of claim 3, but fails to disclose additional circuitry connected to the first stage.

Patel teaches a first inverter (transistors 1050 & 1055) where additional circuitry is in parallel (1068, 1070, 1072, 1074) to the first inverter stage (1050 & 1055), the additional circuitry receiving first and second control signals (PGM1 & PGM2) for selectively controlling the respective pull up path (PMOS 1068) and pull down path (NMOS 1074) of the first inverting stage (1050 & 1055), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the combination disclosed in claim three with the additional circuitry as taught by Patel for adjusting the switching threshold of the buffer circuit.

Regarding claim 10, the combination discloses where a first and second POS device (1068 & 1070) connected in parallel to the pull up path (1050) of the first inverting stage (1050 & 1055), the first PMOS device connected (1068) connected to a supply voltage (Vdd) and a drain connected to the second PMOS device (1070), the drain of the second PMOS device connected to the output of the first inverter (Patel.

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Fig. 10F); first and second NMOS devices (1072 & 1074) connected in parallel to the pull down path of the first inverting stage (1050 & 1055), the first NMOS device having a drain connected to the output of the first inverting stage (Fig. 10F) and a source connected to the drain of the second NMOS device (1074), the source of the second NMOS device being connected to ground (GND).

The Patel reference discloses where the first and second PMOS devices are connected to the control signal (PGM1) and the input signal (In), respectively. Similarly the first and second NMOS devices are connected to the input signal (In) and the control signal (PGM2) respectively. While the connections for each pair of PMOS and NMOS devices disclosed in the reference are opposite of the claim the MPEP 2144.04 VI. C (Rearrangement of Parts) states that it would have been obvious to one of ordinary skill in the art at the time of invention to switch the control signals of the NMOS devices and NMOS devices respectively, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*. 86 USPQ 70.

Claims 13-14 rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (US Pat. 5,612,630) in view of Khellah et al. (US Pat. 6,784,688).

Regarding claim 13, Wright discloses that of claim 1 but fails to show the signal wire as part of an on chip bus line.

Khellah discloses bus lines (Fig. 2) which include repeaters (311-314) or receiver circuit having a buffer circuit (col. 2, line 57, inverters are buffers) therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the

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buffer circuit of Wright and the repeater bus circuit as taught by Khellah for improving signal transmission quality through a system bus.

Regarding claim 14, the combination discloses having repeater circuits (Khellah, 311-314 @ Fig. 3) connected in a point-to-point arrangement.

Allowable Subject Matter

Claims 7, and 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 7, where the switching threshold is dynamically controlled for a predetermined period of time, using first and second aggressor signals, which are, delayed versions of the aggressor signals received from corresponding aggressor signal wires.

Regarding claim 11, where the selection logic for providing the control signals according to the following equations:

$$X = \overline{Vin} \cdot Agg1 \cdot Agg2$$

$$Y = \overline{Vin} + Agg1 + Agg2$$

where Vin is the input signal, and Agg1 and Agg2 are the first and second aggressor signals.

Regarding claim 12, where the selection logic is implemented to meet the following delay criteria:

$$T_{CLK} > T_{SI} > \delta_{max}$$

where T_{CLK} is the clock period, T_{SI} is the delay of the selection logic, and δ_{max} is the maximum difference between the delay of the signal input and the aggressor signals.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dylan White whose telephone number is (571) 272-1406. The examiner can normally be reached on m-f 7:30- 4:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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PRIMARY EXAMINER